loading the second data bit comprises loading the second data bit into the slave latch when the power attains the predetermined level.

39. The method of claim 35 wherein:

latching the first data bit comprises latching the first data bit in the master latch when the power attains the predetermined level; and

loading the first data bit into the slave latch comprises loading the first data bit into the slave latch when the power attains the predetermined level.

REMARKS

Claims 1 - 39 are pending in this broadening reissue application. The Applicant's attorney has amended claims 18-19, 22-27, 31-35, and 38-39. As discussed below, all of the claims are in condition for allowance.

Descrepancy In The Number Of Claims Pending

The Applicant's attorney points out that claims 1-39 are pending, not claims 18-37 as indicated in the office action. The claims 18-39 are included above, in proper reissue format, for the examiner's convenience, and the original claims 1-17 are in the 5,767,709 patent.

Amendments To The Drawings

The Applicant's attorney has amended the figures per the enclosed request for drawing change to correct typographical errors. But these amendments add no new matter to the patent application.

Objection To The Specification Under 35 U.S.C. § 132

The Applicant's attorney has deleted some of the previously added subject matter, and believes that after the examiner reads the below description of an embodiment of the invention, he will understand that the remaining added subject matter is inherent from the original drawings and written description in the '709 patent, an thus is not new matter.

Rejection Of Claims 18-37 Under 35 U.S.C. § 112

The Applicant's attorney has amended some of the claims, and below provides a description of an embodiment of the invention to assist the examiner in understanding the claims. Therefore, in light of these amendments, the Applicant's attorney requests that the examiner withdraw his rejection of the claims.

Description Of An Embodiment Of The Invention

In general, one embodiment of the invention allows an integrated circuit (IC), such as a memory, to latch data during a test mode without an external clock signal. By eliminating the external clock signal, a tester device can access fewer pins of the IC, and thus may increase the testing throughput by testing more ICs at once.

Two tests for memory ICs or ICs that include memory (hereinafter "memory IC") are the memory-cell stress test and the periphery stress test. During the memory-cell stress test, all the memory cells are simultaneously enabled and stressed by simultaneously enabling all of the word lines (rows) and column lines and driving voltages onto both the bit and bit complement lines. Conversely, during the periphery stress test, all of the word lines and column lines are simultaneously disabled.

Each memory IC is designed such that by externally applying predetermined signals to the pins of the IC, a tester can cause the IC to enter the memory-cell or periphery stress test on power up of the IC. Entering a test mode on power up is typically preferred because it reduces the chances that a customer's system will inadvertently enter a test mode while the IC is operating in a non-test mode.

For example purposes, a periphery stress test is discussed in detail with reference to the written specification of the '709 patent and the enclosed amended drawings.

Referring to FIG. 6, because no word lines are enabled during a periphery stress test, both of the signals Local Word Line Odd and Local Word Line Even are inactive logic 0 during the test. Tracing the signal paths back to FIG. 5, this means that both Row Driver Line Even* and Row Driver Line Odd* are inactive logic 1, which means that Row Signal Odd* and Row Signal Even* also are inactive logic 1. Tracing the signal path back to FIG.4 and through the inverters 146 and 142, this means that Row Address Odd* is also inactive logic 1 (circuitry for generating Row Signal Even* from

Row Address Even* (FIG. 3) is similar to the circuitry shown in FIG. 4). Therefore, Row Address Even* is also inactive logic 1.

Referring to FIG. 3, during normal operation of the IC, the pass gate 120 is electrically closed (conducting) such that Row Address Odd* and Row Address Even* always have complementary values, thus insuring that only one word line in an odd/even word-line pair is active at any one time.

But during a peripheral stress test, the pass gate 120 is electrically open (non-conducting) and Row Address Even* is driven to an inactive logic 1 with Rows On and Rows Off*.

Also during the peripheral stress test, the tester drives Row Signal Odd* (FIG. 4) to an inactive logic 1 by simulating an external clock signal and using master and slave latches as discussed below.

Referring to FIGS. 2 – 4, to drive Row Signal Odd* to an inactive logic 1, the tester drives Row Address Odd* to an inactive logic 1 by driving the node 98 (FIG. 2) to a logic 0. To drive node 98 to a logic 0, the tester causes the TTL cell 22 (FIG. 2) to drive the node 72 to a logic 0. Referring to FIG. 1a, which is a schematic diagram of the TTL cell 22 of FIG. 2, the tester drives the node 72 to a logic 0 (regardless of the value of In on the node 15) by driving both Control and Control* to a logic 1.

Next, the tester latches the logic 0 on node 98 with the master latch 95 and latches the inactive logic 1 for Row Signal Odd* with the slave latch (formed by the inverters 146 and 148 of FIG. 4) by generating Clock Derivative on the node 38 (FIGS. 1 and 2) and Smart Clock on the node 132 (FIG. 4). Because Smart Clock is generated in response to the rising edge of Clock Derivative (col. 6, lines 26-27), the focus of the discussion is on the generation of Clock Derivative.

As stated above, the tester does not provide the external signal Clock on the node 12 during the peripheral stress test. Consequently, the tester simulates the external Clock using Control, Control*, and Power-On Reset. When a supply voltage is first applied to the IC, Power-On Reset is an active logic 1, which causes circuitry on the IC to have respective known states. Once the supply voltage attains a predetermined steady-state value (*e.g.*, 3.3 Volts) or a predetermined time thereafter, Power-On Reset transitions to an inactive logic 0, thus releasing the circuitry from the reset condition.

When Control and Control* are logic 1 (to drive nodes 72 and 98 to logic 0 as discussed above) and Power-On Reset is logic 1, the logic in FIG. 1 drives the nodes 3

and 4 (Control' and Control'*, respectively, of FIG. 1a) to logic 0, which causes the TTL Cell 22 (FIGS. 1 and 1a) to drive Clock Derivative to logic 0. Consequently, referring to FIG. 2, Clock Derivative closes the pass gate 90 and thus loads the logic 0 from the node 72 into the master latch 95 such that the node 98 is also at logic 0 as desired per above. Furthermore, referring to FIG. 4, because Smart Clock is logic 0, the pass gate 144 is open, thus preventing loading of the slave latch 146/148.

Next, when Power-On Reset transitions to a logic 0 (Control and Control* remain at logic 1), the logic of FIG. 1 drives the nodes 3 and 4 to a logic 1. This causes the TTL cell 22 to transition Clock Derivative to a logic 1, which opens the pass gate 90 and closes the pass gate 96 such that the master latch 95 latches the logic 0 on the node 98. Furthermore, in response the transition of Clock Derivative from logic 0 to logic 1, Smart Clock pulses from logic 0 to logic 1, and then back to logic 0. While Smart Clock is a logic 1, the pass gate 144 closes to load the slave latch 146/148 with the desired inactive logic 1 for Row Signal Odd*. When Smart Clock transitions back to logic 0, the gate 144 opens such that the slave latch 146/148 latches the logic 1 for Row Signal Odd*.

Consequently, both Row Signal Odd* and Row Signal Even* (FIG. 5) are inactive logic 1 such that no word lines are enabled, which is the desired state in the peripheral stress test.

Conclusion

In light of the foregoing, claims 1 – 17, 20-21, 28-30, and 36-37 as previously pending, and claims 18-19, 22-27, 31-35, and 38-39 as amended are in condition for full allowance, and that action is respectfully requested.

If the Examiner believes that a phone interview would be helpful, he is respectfully requested to contact the Applicant's attorney, Bryan Santarelli, at (425) 455-5575.

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Respectfully submitted,

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